Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KAICHI FUKUDA

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Appeal No. 2003-1690
Application 09/635,061

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ON BRIEF

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Before OWENS, MOORE and POTEATE, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the refusal to allow claims 24-29 as amended after final rejection. These are all of the claims remaining in the application.

THE INVENTION

The appellant claims a process for making a thin film transistor comprising depositing a first gate dielectric layer directly onto a semiconductor layer, patterning these layers into

an island shape, and then, prior to depositing a conductive layer and patterning the conductive layer to form a gate electrode, depositing a second dielectric layer which covers the first dielectric layer. Claim 24 is illustrative:

24. A process for manufacturing a thin film transistor comprising the steps of:

depositing a semiconductor layer on a substrate by using a plasma CVD method;

depositing a first gate dielectric layer consecutively to the step of depositing said semiconductor layer by using the plasma CVD method;

patterning said semiconductor layer together with said first gate dielectric layer into an island shape;

depositing a second gate dielectric layer to cover said first gate dielectric layer patterned into the island shape;

depositing a conductive layer over said second gate dielectric layer; and

patterning said conductive layer to form a gate electrode.

THE REFERENCES

Ipri	4,758,529	Jul. 19, 1988
Lee et al. (Lee)	5,677,206	Oct. 14, 1997 (filed Feb. 26, 1996)
Nam et al. (Nam)	5,693,546	Dec. 2, 1997 (filed Jun. 6, 1996)
Makita et al. (Makita)	5,851,860	Dec. 22, 1998 (filed Jun. 2, 1995)

THE REJECTIONS

The claims stand rejected under 35 U.S.C. § 103 as follows: claims 24 and 26 over Makita in view of Ipri; claims 25 and 27 over Makita in view of Ipri and Nam; and claims 28 and 29 over Makita in view of Ipri and Lee.

OPINION

We reverse the aforementioned rejections. We need to address only the sole independent claim, i.e., claim 24.[1]

The examiner relies upon Makita's disclosure related to figures 7A-7F (answer, page 5). In this disclosure Makita sets forth a process for manufacturing a thin film transistor, comprising depositing a semiconductor layer (503) on a substrate (501, covered by silicon oxide film 502) by plasma CVD (col. 28, lines 55-56), depositing a gate dielectric layer (507) by plasma CVD consecutively to the step of depositing the semiconductor layer (col. 28, lines 48-54), patterning the semiconductor layer together with the gate dielectric layer into an island shape (col. 29, lines 52-57; figure 7D), depositing a conductor layer over the gate dielectric layer, and patterning

[1] The examiner does not rely upon Nam or Lee for a disclosure which remedies the deficiency in Makita and Ipri as to claim 24.

the conductive layer to form a gate dielectric (508; col. 30, lines 1-4; figure 7E). Makita does not disclose the appellant's second gate dielectric layer.

Ipri discloses that in the prior art, when a monocrystalline silicon island (116) was formed on a sapphire wafer (112), and then a silicon dioxide gate dielectric layer (118) was formed on the silicon island by thermal oxidation of the silicon island, there was significant thinning (122, figure 1) of the silicon dioxide layer at the boundary between the silicon island and the wafer surface (114) (col. 2, lines 40-47). Ipri teaches that this thinning degrades the dielectric strength of the gate dielectric by about 67% (col. 2, lines 47-51).

One prior art approach disclosed by Ipri for overcoming this problem was to deposit a polycrystalline silicon layer by standard deposition techniques over a silicon island (216) and the exposed substrate surface (214), and then completely thermally oxidize the polycrystalline silicon layer to form a silicon dioxide gate dielectric layer (218) (col. 2, line 64 - col. 3, line 4). Ipri teaches that "[s]ince the structure of the device **210** [formed by the second discussed prior art process] does not incorporate the thin dielectric regions **122** of device **110** [formed by the first discussed prior art process], it

was expected that a significantly better dielectric strength would be exhibited for this structure. However, the resulting dielectric strength was only marginally better than that of device **110**" (col. 3, lines 4-9).

In Ipri's disclosed prior approach to improving dielectric strength relied upon by the examiner (answer, page 5), a silicon dioxide layer (417) was formed by thermally oxidizing the surface of a silicon island (416), and a layer of silicon nitride (419) was deposited over that layer and over the exposed portions of the wafer surface (414) to provide the desired gate dielectric thickness (T, figure 4) on the silicon island (col. 3, line 53 - col. 4, line 1). Ipri teaches that "[a]lthough the structure **410** [formed by the prior art process relied upon by the examiner] also presents an improvement in dielectric strength compared to the devices **110** and **210**, "it is inherently more unreliable due to the presence of a gate dielectric which comprises two dissimilar materials" (col. 4, lines 4-8).[2]

[2] Ipri's approach to improving the dielectric strength is to form a silicon island on an insulating substrate, thermally oxidize the surface of the silicon island to form a silicon dioxide layer thereon, depositing a silicon layer on the oxidized island and the exposed portion of the substrate surface, and oxidizing the entire silicon layer to form a silicon dioxide layer that covers the island and the exposed wafer surface (col. 4, lines 28-55; figures 5A-E).

The examiner argues that "[i]t would have been obvious to one of ordinary skill in the art at the time of the present invention to use the 2nd gate dielectric layer of Ipri to cover the 1st dielectric layer patterned into an island shape in the process of Makita in order to form a thin-film transistor with improved dielectric strength as is stated by Ipri in column 3, lines 53-55)" (answer, page 5).

The improved dielectric strength in Ipri's prior art embodiment relied upon by the examiner is an improvement over the low dielectric strength of a layer formed by thermal oxidation. The improvement is obtained by depositing a silicon nitride layer over the thermal oxidation layer. Makita's device does not have an oxide layer formed by thermal oxidation and, therefore, does not have the low dielectric strength problem which Ipri's prior art relied upon by the examiner overcomes. Makita's device has only one gate dielectric layer, but it is a deposited layer like the silicon nitride layer Ipri forms to increase the dielectric strength.

The examiner argues as though Ipri would have indicated to one of ordinary skill in the art that two deposited gate dielectric layers are better than one. The examiner, however,

has not pointed out, and it is not apparent, where one of ordinary skill in the art would have found such an indication in Ipri.

For the above reasons we conclude that the examiner has not carried the burden of establishing a *prima facie* case of obviousness of the appellant's claimed invention.

DECISION

The rejections under 35 U.S.C. § 103 of claims 24 and 26 over Makita in view of Ipri, claims 25 and 27 over Makita in view of Ipri and Nam, and claims 28 and 29 over Makita in view of Ipri and Lee, are reversed.

REVERSED

TERRY J. OWENS Administrative Patent Judge	)	
JAMES T. MOORE Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LINDA R. POTEATE Administrative Patent Judge	)	

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